REMARKS

- Claims 30-49, 60-63, 65-78, 89-115, and 118-166 are pending.
- Claims 63, 65, 66, and 96 have been amended in this response.
- Claims 127-166 are newly added in this response.

A clean copy of the pending claims are attached for the Examiner's convenience.

The Applicant appreciates that the Examiner has attempted to carefully review the many references submitted by the Applicant in the various IDSs in this case, and has initialed the various form 1449s, with the exception of references C77 and C78. As the undersigned does not have a translated copy of these two references and does not know of any particular materiality of those references, and as those references contain dates which post-date Applicant's priority date, Applicant submits that it is unnecessary to submit translated versions of those references. In other words, it is fine that the Examiner has not initiated off on those references, and Applicant would suggest that it is reasonable for the Examiner not to consider them further.

The Examiner has rejected various claims as anticipated or obvious in light of USP 5,312,518 ("Kadomura"). The Examiner has also allowed the subject matter of various claims, and specifically those discussed below.

In the spirit of advancing this application, Applicant has herein amended its claims to encompass subject matter understood to be allowable by the Examiner. The Applicant does not

agree that the subject matter not allowed is unpatentable, but has chosen to take up that matter in a continuation application to be subsequently filed.

The following points are worthy of note:

- Independent claim 30 and its dependent claims, which have been allowed by the Examiner, remain unchanged.

- Independent claim 63 has been amended to include the limitation of previous claim 64 (now canceled), which was deemed to contain allowable subject matter by the Examiner.

- Independent claim 96 has been amended to include the limitation that "the etch environment comprises a fluorohydrocarbon, wherein the fluorohydrocarbon contains at least as many hydrogen atoms as fluorine atoms." Given the Examiner's allowance of claim 97 (which contains the limitation "wherein the etch environment comprises a first gas selected from the group comprising CH_3F and CH_2F_2"), a limitation obviously not present in Kadomura,[1] Applicant assumes that claim 96 as amended would contain allowable subject matter.

- New independent claim 127 comprises the subject matter of previous claim 75, which was allowed by the Examiner.

- New independent claim 150 comprises the subject matter of previous claim 106, which was allowed by the Examiner.

In summary, each of the independent claims now recite subject matter expressly (or by logical inference) deemed allowable by the Examiner. With the subject matter of all pending independent claims being allowable in light of the prior art, it necessarily follows that all claims (including their dependent claims) are allowable.

[1] As the Examiner will appreciate, Kadomura deals with etchants which include sulphur, which are clearly not fluorohydrocarbons.

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Therefore, Applicant submits that pending claims 30-49, 60-63, 65-78, 89-115, and 118-166 are patentable, and requests the issuance of a Notice of Allowance.

Respectfully submitted,

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1-29. (canceled)

30. (previously presented) A method of etching a semiconductor wafer comprising a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the silicon oxide layer in an etchant environment comprising a fluorohydrocarbon, wherein the fluorohydrocarbon contains at least as many hydrogen atoms as fluorine atoms, and wherein the etchant environment provides silicon oxide-to-silicon nitride selectivity.

31. (previously presented) The method of claim 30, wherein the fluorohydrocarbon is CH_3F.

32. (previously presented) The method of claim 30, wherein the fluorohydrocarbon contains the same number of hydrogen and fluorine atoms.

33. (previously presented) The method of claim 32, wherein the fluorohydrocarbon is CH_2F_2.

34. (previously presented) The method of claim 30, wherein the etchant environment further comprises a fluorinated gas.

35. (previously presented) The method of claim 34, wherein the fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

36. (previously presented) The method of claim 34, wherein the etchant environment further comprises an inert gas.

37. (previously presented) The method of claim 36, wherein the inert gas is argon.

38. (previously presented) The method of claim 30, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

39. (previously presented) The method of claim 30, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

40. (previously presented) The method of claim 30, wherein the silicon nitride layer is formed with an uneven topography.

41. (previously presented) The method of claim 30, wherein the semiconductor wafer further comprises two conductors, wherein the silicon nitride layer is formed above the conductors, and wherein the plasma etching forms an opening in the silicon oxide between the conductors.

42. (previously presented) The method of claim 30, further comprising heating the semiconductor wafer during plasma etching.

43. (previously presented) The method of claim 42, wherein the semiconductor wafer is heated to between about 20 and 80 degrees C.

44. (previously presented) The method of claim 42, wherein the semiconductor wafer is heated to between about 30 and 60 degrees C.

45. (previously presented) The method of claim 42, wherein the semiconductor wafer is heated to between about 35 and 50 degrees C.

46. (previously presented) The method of claim 42, wherein the semiconductor wafer is heated by heating an electrode adjacent to the semiconductor wafer.

47. (previously presented) The method of claim 46, wherein the electrode is heated to between about 20 and 80 degrees C.

48. (previously presented) The method of claim 46, wherein the electrode is heated to between about 30 and 60 degrees C.

49. (previously presented) The method of claim 46, wherein the electrode is heated to between about 35 and 50 degrees C.

50-59. (canceled)

60. (previously presented) The method of claim 30, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 10-to-1.

61. (previously presented) The method of claim 30, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

62. (previously presented) The method of claim 30, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

63. (currently amended) A method of etching a semiconductor wafer comprising a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the semiconductor wafer in an etchant environment, wherein the method comprises heating the semiconductor wafer during plasma etching to increase the silicon oxide-to-silicon nitride selectivity, wherein the etchant environment comprises a fluorohydrocarbon, wherein the fluorohydrocarbon contains at least as many hydrogen atoms as fluorine atoms.

64. (canceled)

65. (currently amended) The method of claim 63, wherein the fluorohydrocarbon is CH_3F.

66. (currently amended) The method of claim 63, wherein the fluorohydrocarbon contains the same number of hydrogen and fluorine atoms.

67. (previously presented) The method of claim 66, wherein the fluorohydrocarbon is CH_2F_2.

68. (previously presented) The method of claim 63, wherein the etchant environment further comprises a fluorinated gas.

69. (previously presented) The method of claim 68, wherein the fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

70. (previously presented) The method of claim 68, wherein the etchant environment further contains an inert gas.

71. (previously presented) The method of claim 70, wherein the inert gas is argon.

72. (previously presented) The method of claim 63, wherein the semiconductor wafer is heated to between about 20 and 80 degrees C.

73. (previously presented) The method of claim 63, wherein the semiconductor wafer is heated to between about 30 and 60 degrees C.

74. (previously presented) The method of claim 63, wherein the semiconductor wafer is heated to between about 35 and 50 degrees C.

75. (previously presented) The method of claim 63, wherein the semiconductor wafer is heated by heating an electrode adjacent to the semiconductor wafer.

76. (previously presented) The method of claim 75, wherein the electrode is heated to between about 20 and 80 degrees C.

77. (previously presented) The method of claim 75, wherein the electrode is heated to between about 30 and 60 degrees C.

78. (previously presented) The method of claim 75, wherein the electrode is heated to between about 35 and 50 degrees C.

79-88. (canceled)

89. (previously presented) The method of claim 63, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 10-to-1.

90. (previously presented) The method of claim 63, wherein the silicon oxide-to-silicon nitride selectivity is greater than 20-1.

91. (previously presented) The method of claim 63, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

92. (previously presented) The method of claim 63, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

93. (previously presented) The method of claim 63, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

94. (previously presented) The method of claim 63, wherein the silicon nitride layer is formed with an uneven topography.

95. (previously presented) The method of claim 63, wherein the semiconductor wafer further comprises two conductors, wherein the silicon nitride layer is formed above the conductors, and wherein the plasma etching forms an opening in the silicon oxide between the conductors.

96. (currently amended) A method of etching a semiconductor wafer containing a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the semiconductor wafer using an etch environment that provides a silicon oxide-to-silicon nitride selectivity of greater than or equal to 10-to-1, wherein the etch environment comprises a fluorohydrocarbon, wherein the fluorohydrocarbon contains at least as many hydrogen atoms as fluorine atoms.

97. (previously presented) The method of claim 96, wherein the etch environment comprises a first gas selected from the group comprising CH_3F and CH_2F_2.

98. (previously presented) The method of claim 97, wherein the etch environment further comprises a second fluorinated gas.

99. (previously presented) The method of claim 98, wherein the second fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

100. (previously presented) The method of claim 98, wherein the etch environment further comprises an inert gas.

101. (previously presented) The method of claim 100, wherein the inert gas is argon.

102. (previously presented) The method of claim 96, further comprising heating the semiconductor wafer during plasma etching.

103. (previously presented) The method of claim 102, wherein the semiconductor wafer is heated to between about 20 and 80 degrees C.

104. (previously presented) The method of claim 102, wherein the semiconductor wafer is heated to between about 30 and 60 degrees C.

105. (previously presented) The method of claim 102, wherein the semiconductor wafer is heated to between about 35 and 50 degrees C.

106. (previously presented) The method of claim 102, wherein the semiconductor wafer is heated by heating an electrode adjacent to the semiconductor wafer.

107. (previously presented) The method of claim 106, wherein the electrode is heated to between about 20 and 80 degrees C.

108. (previously presented) The method of claim 106, wherein the electrode is heated to between about 30 and 60 degrees C.

109. (previously presented) The method of claim 106, wherein the electrode is heated to between about 35 and 50 degrees C.

110. (previously presented) The method of claim 97, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

111. (previously presented) The method of claim 97, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

112. (previously presented) The method of claim 97, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 50-to-1.

113. (previously presented) The method of claim 102, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

114. (previously presented) The method of claim 102, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

115. (previously presented) The method of claim 96, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

116-117. (canceled)

118. (previously presented) The method of claim 96, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

119. (previously presented) The method of claim 96, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 50-to-1.

120. (previously presented) The method of claim 96, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

121. (previously presented) The method of claim 96, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

122. (previously presented) The method of claim 96, wherein the silicon nitride layer is formed with an uneven topography.

123. (previously presented) The method of claim 96, wherein the semiconductor wafer further comprises two conductors, wherein the silicon nitride layer is formed above the conductors, and wherein the plasma etching forms an opening in the silicon oxide between the conductors.

124. (previously presented) The method of claim 41, wherein the conductors are comprised of polysilicon.

125. (previously presented) The method of claim 95, wherein the conductors are comprised of polysilicon.

126. (previously presented) The method of claim 123, wherein the conductors are comprised of polysilicon.

127. (new) A method of etching a semiconductor wafer comprising a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the semiconductor wafer in an etchant environment, wherein the method comprises heating the semiconductor wafer during plasma etching to increase the silicon oxide-to-silicon nitride selectivity, wherein the semiconductor wafer is heated by heating an electrode adjacent to the semiconductor wafer.

128. (new) The method of claim 127, wherein the etchant environment comprises a fluorohydrocarbon, wherein the fluorohydrocarbon contains at least as many hydrogen atoms as fluorine atoms.

129. (new) The method of claim 128, wherein the fluorohydrocarbon is CH_3F.

130. (new) The method of claim 127, wherein the etchant environment comprises a fluorohydrocarbon, wherein the fluorohydrocarbon contains the same number of hydrogen and fluorine atoms.

131. (new) The method of claim 130, wherein the fluorohydrocarbon is CH_2F_2.

132. (new) The method of claim 127, wherein the etchant environment further comprises a fluorinated gas.

133. (new) The method of claim 132, wherein the fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

134. (new) The method of claim 132, wherein the etchant environment further contains an inert gas.

135. (new) The method of claim 134, wherein the inert gas is argon.

136. (new) The method of claim 127, wherein the semiconductor wafer is heated to between about 20 and 80 degrees C.

137. (new) The method of claim 127, wherein the semiconductor wafer is heated to between about 30 and 60 degrees C.

138. (new) The method of claim 127, wherein the semiconductor wafer is heated to between about 35 and 50 degrees C.

139. (new) The method of claim 127, wherein the electrode is heated to between about 20 and 80 degrees C.

140. (new) The method of claim 127, wherein the electrode is heated to between about 30 and 60 degrees C.

141. (new) The method of claim 127, wherein the electrode is heated to between about 35 and 50 degrees C.

142. (new) The method of claim 127, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 10-to-1.

143. (new) The method of claim 127, wherein the silicon oxide-to-silicon nitride selectivity is greater than 20-1.

144. (new) The method of claim 127, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

145. (new) The method of claim 127, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

146. (new) The method of claim 127, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

147. (new) The method of claim 127, wherein the silicon nitride layer is formed with an uneven topography.

148. (new) The method of claim 127, wherein the semiconductor wafer further comprises two conductors, wherein the silicon nitride layer is formed above the conductors, and wherein the plasma etching forms an opening in the silicon oxide between the conductors.

149. (new) The method of claim 148, wherein the conductors are comprised of polysilicon.

150. (new) A method of etching a semiconductor wafer containing a silicon oxide layer formed over a silicon nitride layer, the method comprising plasma etching the semiconductor wafer using an etch environment that provides a silicon oxide-to-silicon nitride selectivity of

greater than or equal to 10-to-1, wherein the semiconductor wafer is heated during plasma etching by heating an electrode adjacent to the semiconductor wafer.

151. (new) The method of claim 150, wherein the etch environment comprises a first gas selected from the group comprising CH_3F and CH_2F_2.

152. (new) The method of claim 151, wherein the etch environment further comprises a second fluorinated gas.

153. (new) The method of claim 152, wherein the second fluorinated gas is selected from the group consisting of CF_4 and CHF_3.

154. (new) The method of claim 152, wherein the etch environment further comprises an inert gas.

155. (new) The method of claim 154, wherein the inert gas is argon.

156. (new) The method of claim 150, wherein the electrode is heated to between about 20 and 80 degrees C.

157. (new) The method of claim 150, wherein the electrode is heated to between about 30 and 60 degrees C.

158. (new) The method of claim 150, wherein the electrode is heated to between about 35 and 50 degrees C.

159. (new) The method of claim 150, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 20-to-1.

160. (new) The method of claim 150, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 30-to-1.

161. (new) The method of claim 150, wherein the silicon oxide-to-silicon nitride selectivity is greater than or equal to 50-to-1.

162. (new) The method of claim 150, wherein the silicon oxide layer is formed directly above the silicon nitride layer.

163. (new) The method of claim 150, wherein the silicon oxide is selected from the group consisting of undoped silicon oxide and doped silicon oxide.

164. (new) The method of claim 150, wherein the silicon nitride layer is formed with an uneven topography.

165. (new) The method of claim 150, wherein the semiconductor wafer further comprises two conductors, wherein the silicon nitride layer is formed above the conductors, and wherein the plasma etching forms an opening in the silicon oxide between the conductors.

166. (new) The method of claim 165, wherein the conductors are comprised of polysilicon.